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L5	l4 and (optimiz$ near2 code) and coprocessor	1	L5
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their existing investment to produce better **optimized code** [10]Some profiling methods today utilize
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processor, eventually as optimal as hand-**optimized code**, while cutting down the code development
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the running time of the optimizer, making **optimized code** available sooner. Another side e#ect of
that pairs a normal processor with an optimizing **coprocessor**. This system o#ers potentially significant
opportunities for several reasons. The use of a **coprocessor** allows the optimization process to run in
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high level language to be compiled into well **optimized code**. Hence, data flow optimizations will be one
feature hardware data caches, DSPs often use DMA **coprocessor**(s) combined with general purpose internal data
www.lohier.com/frantz/publications/asset99/asset99v2.pdf

Turboscalar: A High Frequency High IPC Microarchitecture - Bryan Black And (2000) (Correct)
with the VLIW/EPIC machines is that the **code optimized** for a current generation machine may not run
of the object code via an Instruction-Path **Coprocessor** [3]Finally, through dynamic code
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Abstract: There is significant performance motivation to build larger and wider superscalar machines, however the implementation complexity can be overwhelming. When superscalar machines grow they necessarily become deeper in order to maintain frequency. As the pipeline depth increases the performance gained by a wide instruction fetch and dispatch is lost to branch misprediction penalty cycles. This work proposes the new Turboscalar microarchitecture, which is strongly based on the superscalar... (Update)


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